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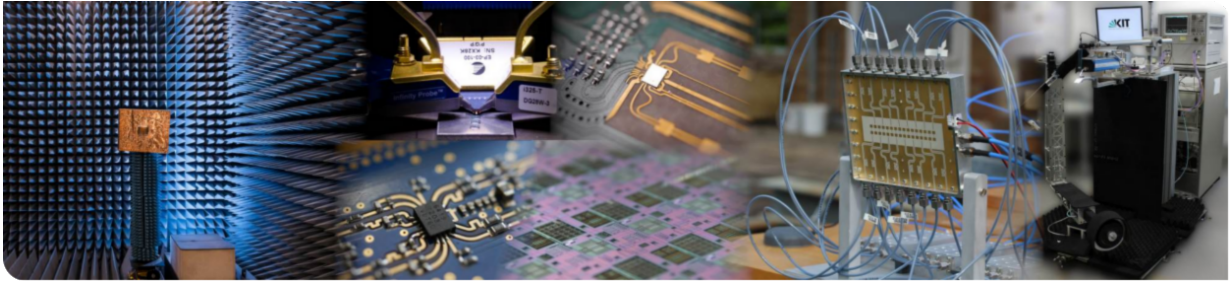
A Broadband Zero-IF Down-Conversion Mixer in 130 nm SiGe BiCMOS for Beyond 5G Communication Systems in D-Band

Andreas Tsouchlos | 10.09.2024



Overview

- Proposed Ideas
- Own Simulations
- Discussion & Conclusion

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- Proposed Ideas
- Own Simulations
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Proposed Design: Overview

- Paper by Maiwald, *et al.* **[Mai+21]**

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A Broadband Zero-IF Down-Conversion Mixer in 130 nm SiGe BiCMOS for Beyond 5G Communication Systems in D-Band

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***Abstract*—This brief presents a broadband D-band down-conversion mixer in a cost efficient 130 nm SiGe BiCMOS technology with a f_t/f_{max} of 250/370 GHz from Infineon Technologies AG. The proposed mixer covers the entire D-band with a 32 dB peak conversion gain and a 3 dB bandwidth of 35 GHz at a measured noise figure between 9.5 and 12 dB in the specified band while consuming only 65 mW DC power. To achieve large RF and IF bandwidths and a low noise figure, the mixer design is based on a low-biased switching quad, which is loaded with a modified Cherry-Hooper transimpedance amplifier. The results, which are verified by measurements, are based on a detailed analysis of the transistor characteristics, broadband matching networks and an appropriate layout parasitic extraction. All interfaces to the circuit are designed single-ended for a dense chip-to-package transition. For this purpose, high performance Marchand baluns are used at RF- and LO-port, respectively. With a moderate noise figure and a low power consumption, the presented circuit meets the requirements for beyond 5G systems.**

***Index Terms*—6G, beyond 5G, broadband, communication, D-band, mixer, receiver.**

Fig. 1. System concept for a broadband phased array receiver with LO-path-phase-shifting.

I. INTRODUCTION

MMWAVE 5G meets the increasing demands of today's modern applications. Here, carrier frequencies between 28 and 40 GHz and sub-channel bandwidths up to 800 MHz are set to enable data-rates up to 10 Gbit/s. Following these trends for high-speed communication systems, the demand on even higher data rates and hence, even larger bandwidths and higher frequencies is already visible [1]. The advances in semiconductor processes with respect to f_t and f_{max} of the transistors, enable an efficient implementations of high performance communication components and systems [2], [3]. According to these trends, frequency bands beyond 100 GHz are promising for future communication systems with data rates on the 100 Gbps order [4]. They do not only offer a moderate atmospheric absorption and a high availability of high aggregate carrier bandwidths but also promote a high degree of integration for area efficient broadband couplers as well as antennas on-chip or efficient antenna-in-package solutions. Furthermore, on-chip transmission lines can be used for broadband matching networks with a reasonable area consumption. Due to a small effective antenna area, that increases free-space losses beyond 100 GHz, systems with high antenna gain and array factors are required for communication over several meters. Increasing array factors lead to smaller antenna beam widths, which need to be steered electronically in order to avoid the need for mechanical alignments between transmitter (TX) and receiver (RX). Consequently, large arrays, including more sub-receiver channels, lead to a high power consumption and heat development. The receiver front-end in Fig. 1, shows an adequate system concept, which is addressing these challenges. It features an array of power-saving

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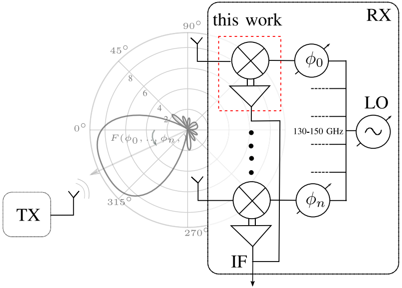
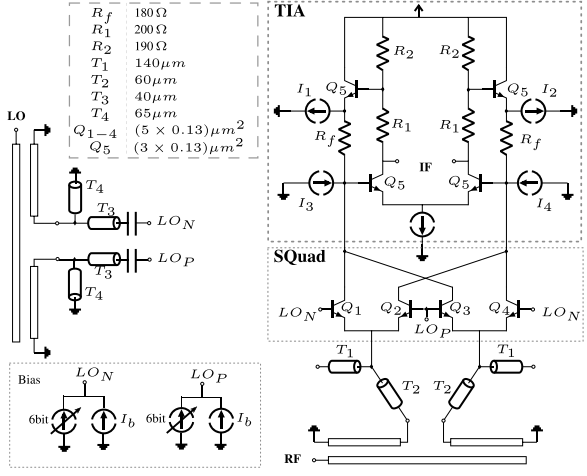


- High bandwidth, low noise figure, low power consumption, small size
- Applicable to electronic beam stearing for mm-Wave
- 130nm SiGe BiCMOS technology from Infineon Technologies AG with f_t/f_{max} of $250/370$ GHz

[Mai+21] T. Maiwald et al., “A Broadband Zero-IF Down-Conversion Mixer in 130 nm SiGe BiCMOS for Beyond 5G Communication Systems in D-Band”, in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 7, pp. 2277-2281, July 2021

Proposed Design: Mixer Core Cell

- Usage of switching quad (SQuad) instead of conventional Gilbert cell for more voltage headroom
- Mixer loaded by modified Cherry-Hooper [CH63] transimpedance amplifier (TIA)
- Transmission line based differential L-type matching networks for high bandwidth
- Signal fed using marchand baluns for high bandwidth

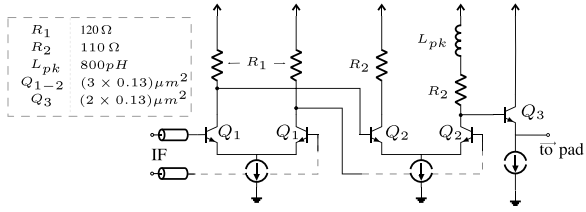


[CH63] E.M. Cherry and D.E. Hooper, "The design of wide-band transistor feedback amplifiers", *Proceedings of the Institution of Electrical Engineers*, vol. 110, pp. 375-389, February 1963

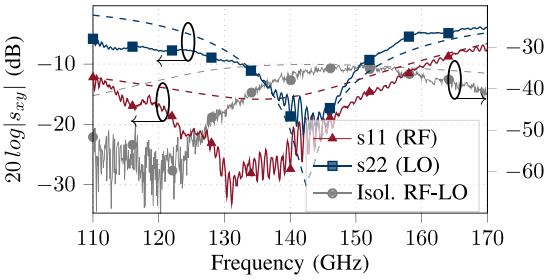
Proposed Design: IF Buffer

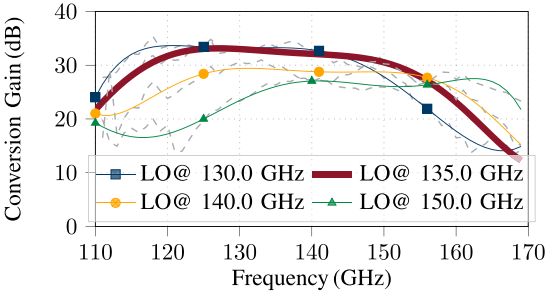
- Three-stages: two differential amplifier stages and an emitter follower
- Includes differential to single-ended conversion enabling dense chip-to-package transition
- Inductive peaking for bandwidth enhancement

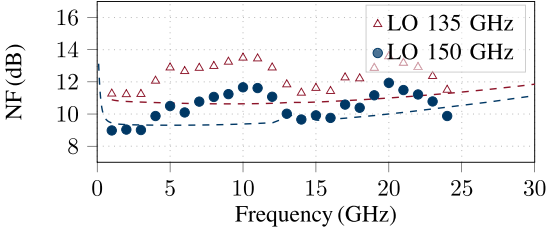
R_1	$120\,\Omega$
R_2	$110\,\Omega$
L_{pk}	$800pH$
Q_{1-2}	$(3 \times 0.13)\mu m^2$
Q_3	$(2 \times 0.13)\mu m^2$

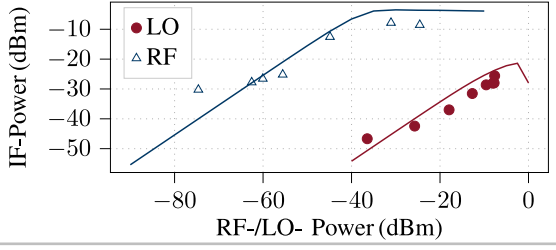


Proposed Design: Simulation/Measurement Results









Overview

- Proposed Ideas
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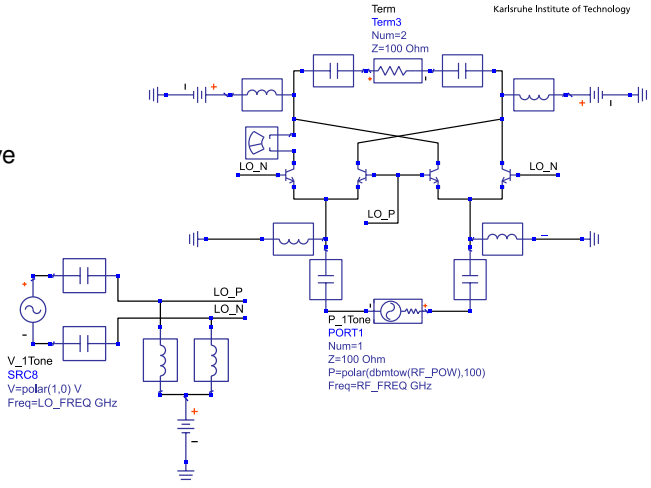
Design Steps

1. Determination of operating point of individual stages
   - SQuad
   - TIA
   - Buffer
2. Integration
   - SQuad & TIA
   - SQuad, TIA & Buffer
3. Further iterative optimization of parameters (e.g., determine LO power, increase buffer current for linearity, . . .)
4. Matching

Operating Point: Switching Quad

- Operation
  - Responsible for actual mixing
  - Multiplication of RF-signal with square wave $\rightarrow$ generation of mixing products at IF-frequency and harmonics

- Determination of operating point
  - Exact value of V_{CE} not crucial
  - V_{BE}: Examination of s_{21} of Large-signal s-parameter simulation and noise figure (analogous to **[Mai+21]**)



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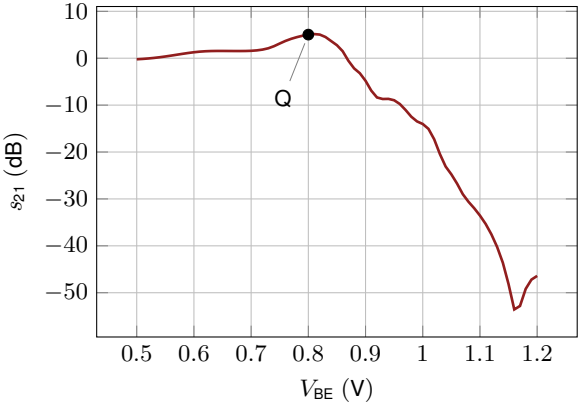
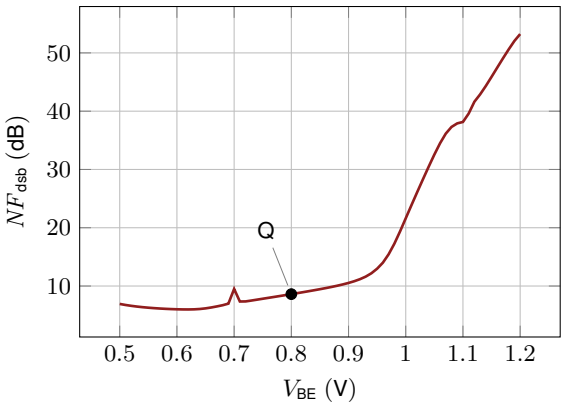
Operating Point: Switching Quad

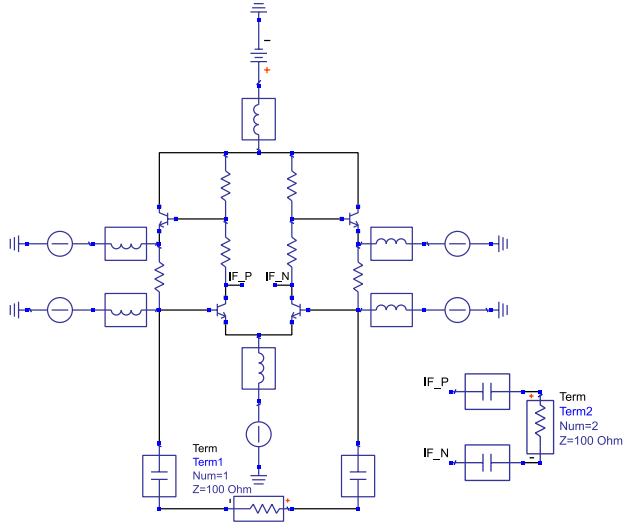




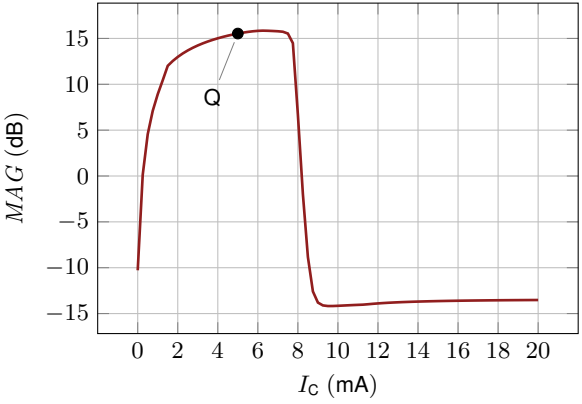
- Plotted for $f_{LO} = 135\,\text{GHz}$, $f_{RF} = 140\,\text{GHz}$
- Double-sideband noise figure NF_{dsb} (direct conversion mixer)
- Chosen operating point: $V_{BE} = 0{,}8\,\text{V}$

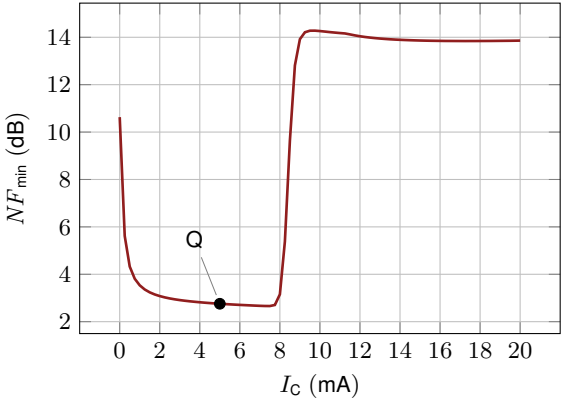
Operating Point: Transimpedance Amplifier

- Operation
  - Conversion of switched current to voltage, amplification
  - Modified Cherry-Hooper topology: decoupling of bandwidth and gain, modification for greater dynamic range
- Determination of operating point
  - Exact value of supply voltage not crucial
  - S-parameter simulation: Examination of maximum available gain (MAG) and minimum noise figure (NF_{min})
  - At this stage: only determination of operating point of bottom transistors



Operating Point: Transimpedance Amplifier

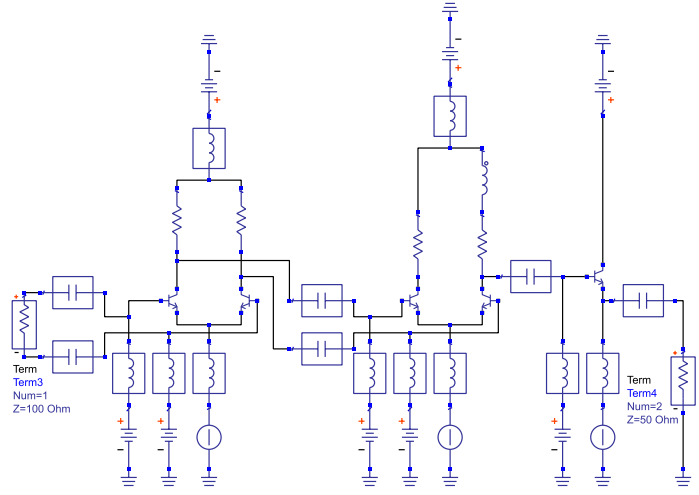




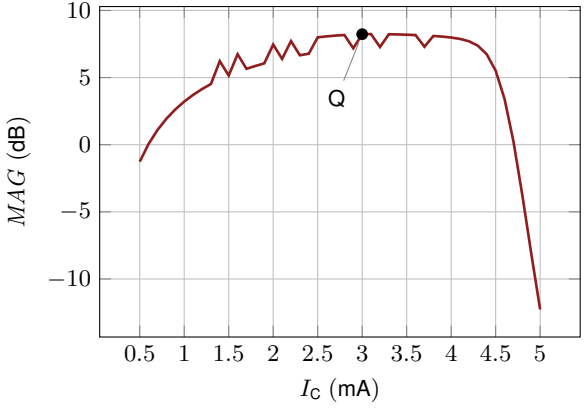
- Plotted for $f_{IF} = 20\,\text{GHz}$
- Chosen operating point: $I_C = 5\,\text{mA}$ (with multiplier of 10)

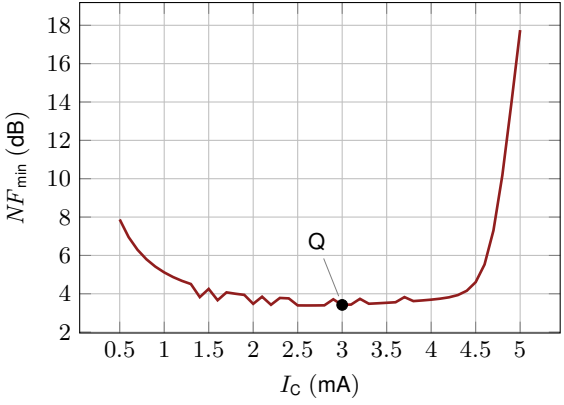
Operating Point: Buffer

- Operation
  - Amplification of signal
  - Comprises three stages: two differential amplifiers and an emitter follower
- Determination of operating point
  - Exact value of supply voltage not crucial at this point
  - S-parameter simulation: Examination of MAG and NF_{min}
  - **Note**: Adjustment with respect to linearity at the very end



Operating Point: Buffer

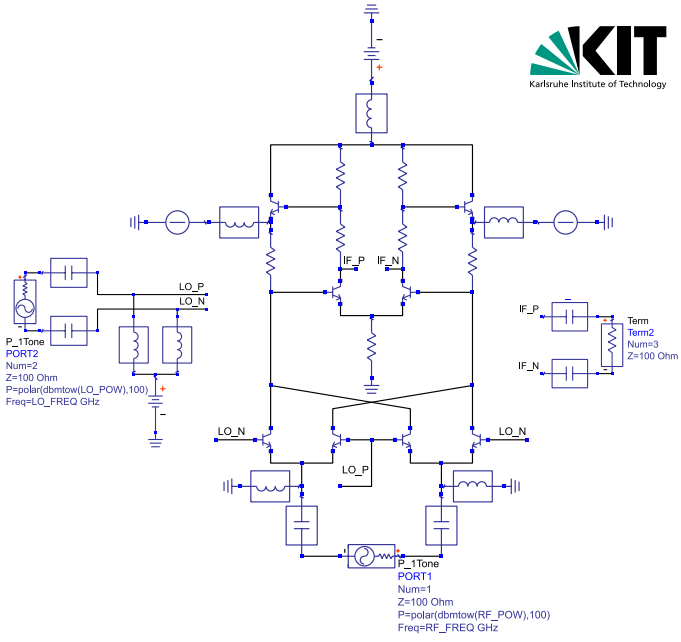




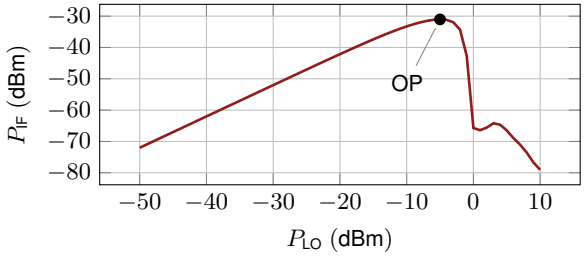
- Plotted for $f_{IF} = 20\,\text{GHz}$
- Chosen operating point: $I_C = 3\,\text{mA}$

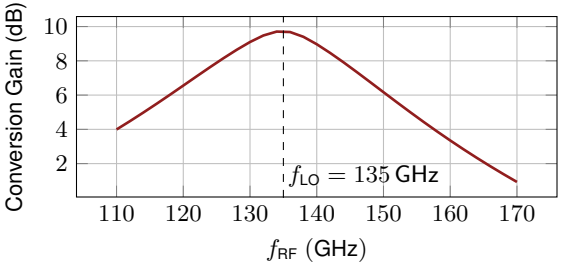
Integration: SQuad & TIA

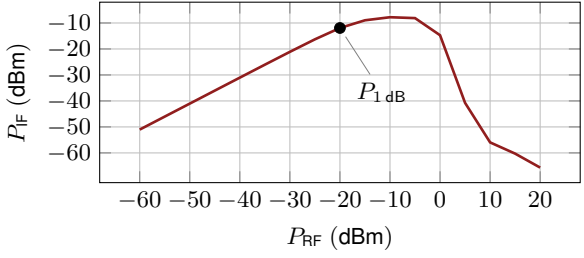
- DC coupling $\rightarrow$ Redesign of bias circuitry
- Supply voltage fixed to $2{,}5\,\mathrm{V}$ to not exceed breakdown voltage of transistors
- Examination using Harmonic-Balance simulation:
  - Conversion gain
  - $1\,\mathrm{dB}$ compression point ($P_{1\,\mathrm{dB}}$)
  - Noise figure

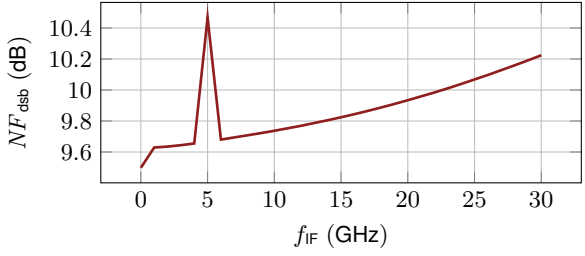


Integration: SQuad & TIA



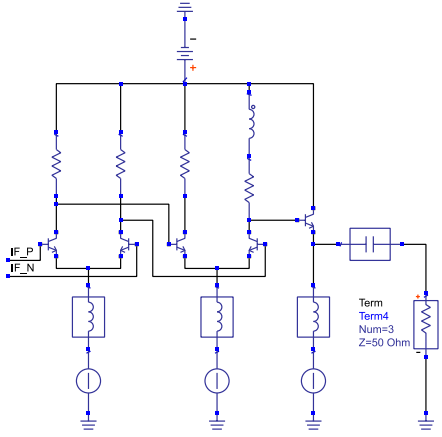






Integration: SQuad, TIA & Buffer

- DC coupling $\rightarrow$ Redesign of bias circuitry
- Supply voltage fixed to $2{,}5\,\mathrm{V}$
- Examination using Harmonic-Balance simulation:
  - Conversion gain
  - $1\,\mathrm{dB}$ compression point ($P_{1\,\mathrm{dB}}$)
  - Noise figure



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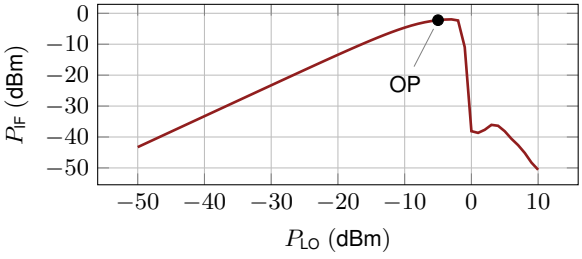
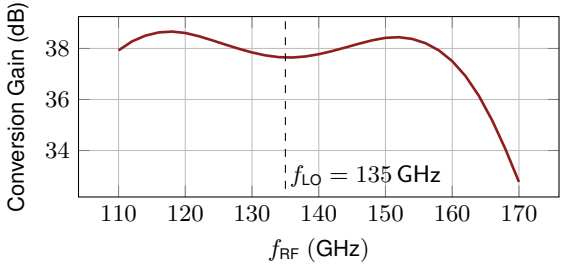
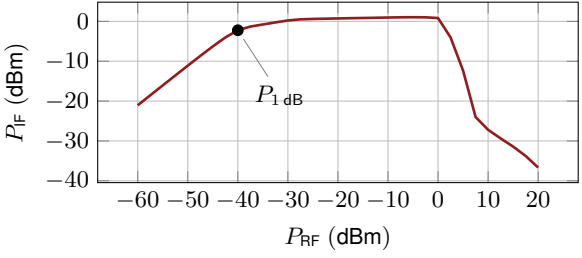
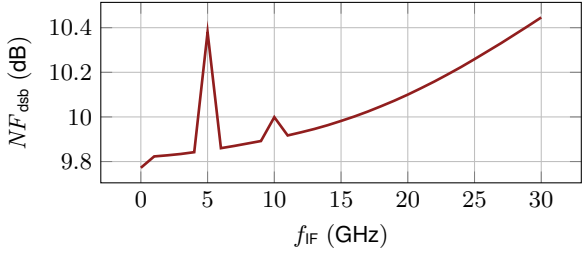
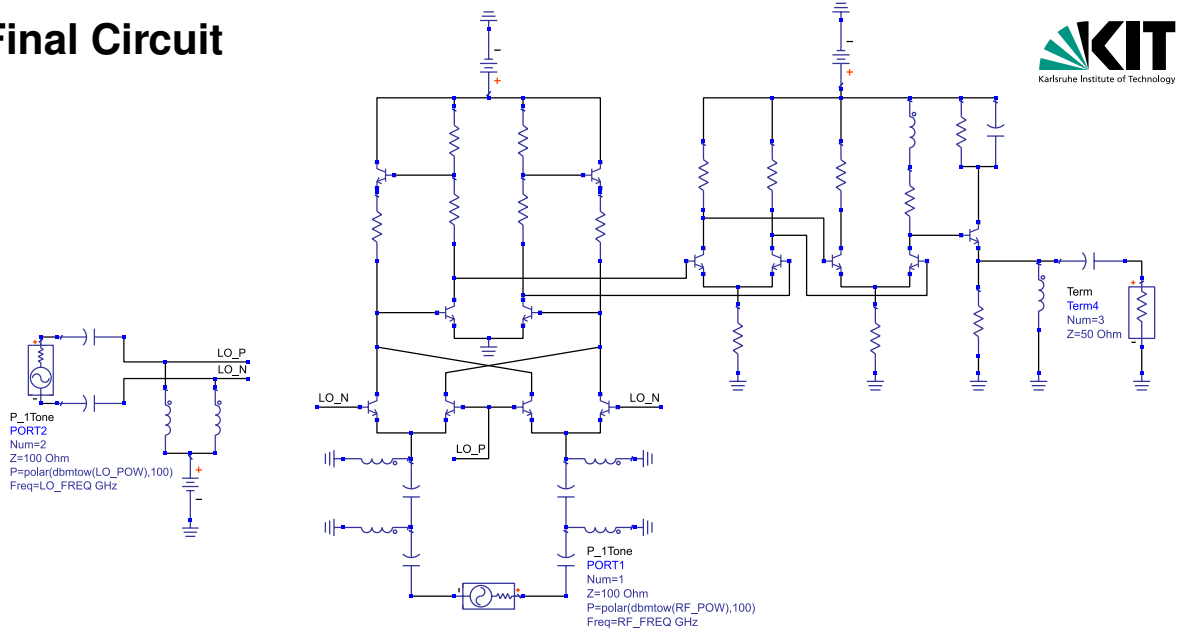








Final Circuit



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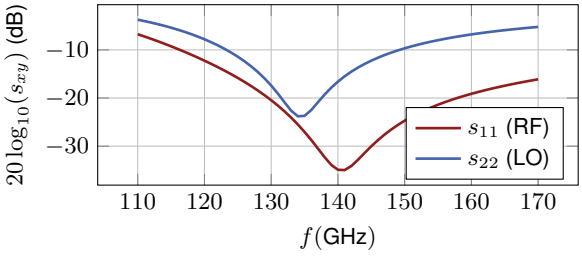

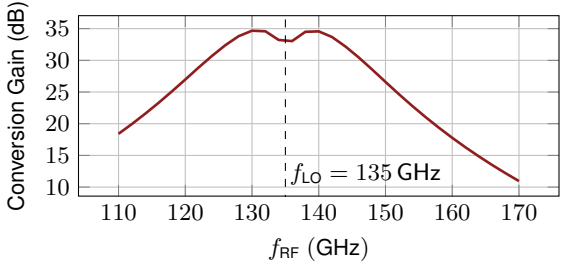

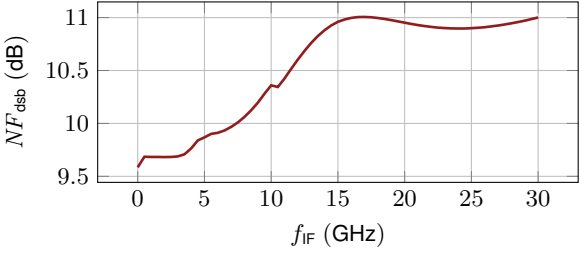

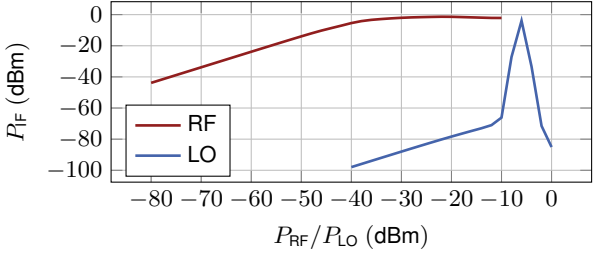

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Discussion & Conclusion

- Own simulations
  - Better results to be expected (technology with higher f_t, f_{max}, stability not considered)
  - Maybe better results by using current mirrors to set operating points of buffer instead of resistors
- General structure
  - Removal of g_m stage of Gilbert cell $\rightarrow$ more voltage headroom
  - High bandwidth TIA and inductive peaking $\rightarrow$ high bandwidth
  - Differential to single-ended conversion $\rightarrow$ dense chip-to-package transition
- Applications of this design
  - SiGe HBT technology integrable with CMOS $\rightarrow$ scalable, suitable for mixed-signal ICs
  - Ideal for electronic beam stearing in mm-Wave applications (because of small size, moderate noise figure)

Questions

Thank you for your attention!
Any questions?