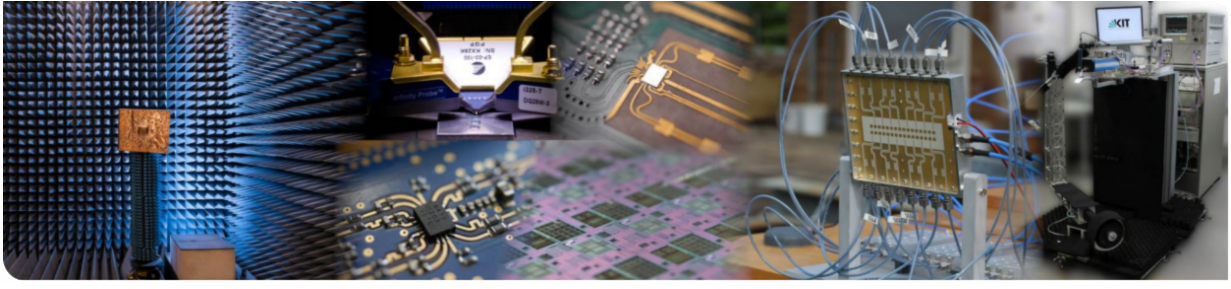
A Broadband Zero-IF Down-Conversion Mixer in 130 nm SiGe BiCMOS for Beyond 5G Communication Systems in D-Band

Andreas Tsouchlos | 10.09.2024



Overview

- Proposed Ideas
- Own Simulations
- Discussion & Conclusion

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Proposed Design: Overview

- Paper by Maiwald, *et al.* **[Mai+21]**

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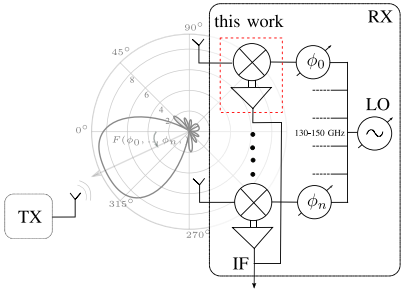
Tim Maiwald[1], Graduate Student Member, IEEE, Julian Fleischer[1], Graduate Student Member, IEEE, Katharina Keller[1], Graduate Student Member, IEEE, Marco Dietz, Graduate Student Member, IEEE, Amelie Hagelauer[1], Senior Member, IEEE, Markus Vossiemer[1], Member, IEEE, and Robert Weigel[1], Fellow, IEEE

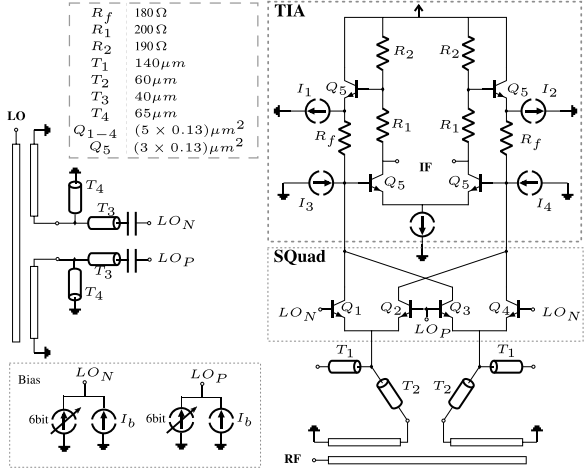


- High bandwidth, low power consumption, small size
- Applicable to electronic beam stearing for mm-Wave
- SiGe BiCMOS technology (B11HFC) from Infineon Technologies AG with f_t/f_{max} of $250/370$ GHz

[Mai+21] T. Maiwald et al., “A Broadband Zero-IF Down-Conversion Mixer in 130 nm SiGe BiCMOS for Beyond 5G Communication Systems in D-Band”, in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 7, pp. 2277-2281, July 2021

Proposed Design: Mixer Core Cell

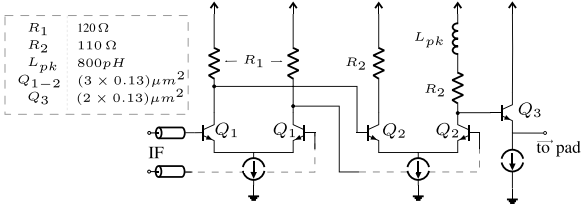
- Usage of switching quad (SQuad) instead of conventional Gilbert cell for more voltage headroom
- Mixer loaded by modified Cherry-Hooper [CH63] transimpedance amplifier (TIA)
- Transmission line based differential L-type matching networks for high bandwidth
- Signal fed using marchand baluns for high bandwidth



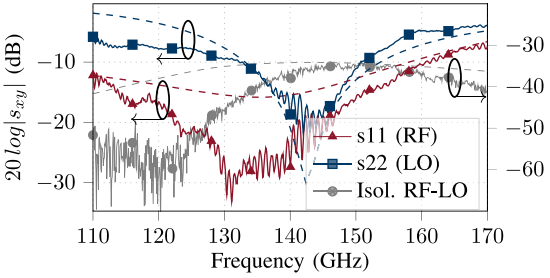
[CH63] E.M. Cherry and D.E. Hooper, "The design of wide-band transistor feedback amplifiers", *Proceedings of the Institution of Electrical Engineers*, vol. 110, pp. 375-389, February 1963

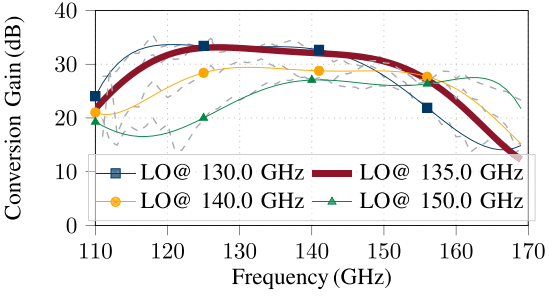
Proposed Design: IF Buffer

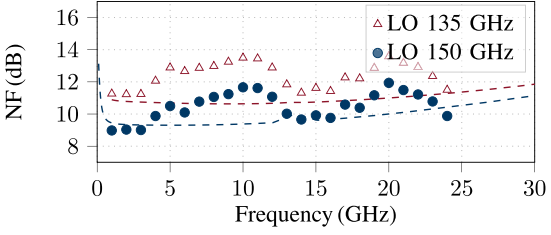
- Three-stages: two differential amplifier stages and an emitter follower
- Includes differential to single-ended conversion enabling dense chip-to-package transition
- Inductive peaking for bandwidth enhancement

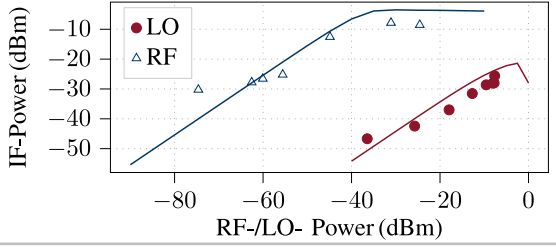


Proposed Design: Simulation/Measurement Results









Overview

- Proposed Ideas
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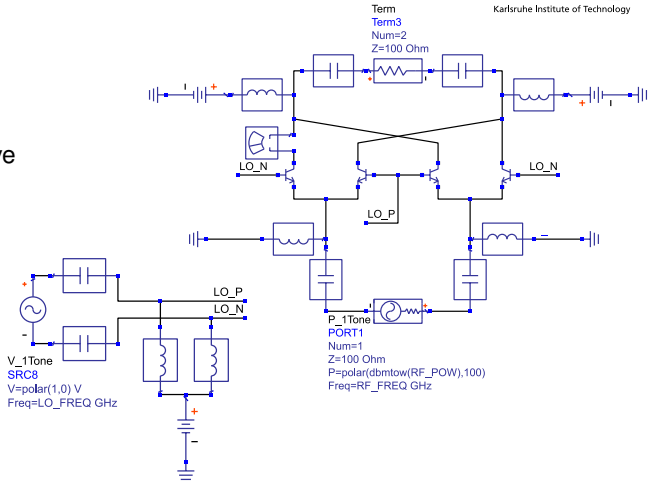
Design Steps

1. Determination of operating point of individual stages
   - SQuad
   - TIA
   - Buffer
2. Integration
   - SQuad & TIA
   - SQuad, TIA & Buffer
3. Further iterative optimization of parameters (e.g., determine LO power, increase buffer current for linearity, . . .)
4. Matching of input and output

Operating Point: Switching Quad

- Operation
  - Responsible for actual mixing
  - Multiplication of RF-signal with square wave $\rightarrow$ generation of mixing products at IF-frequency and harmonics

- Determination of operating point
  - Exact value of V_{CE} not crucial
  - V_{BE}: Examination of s_{21} of Large-signal s-parameter simulation and noise figure (analogous to **[Mai+21]**)



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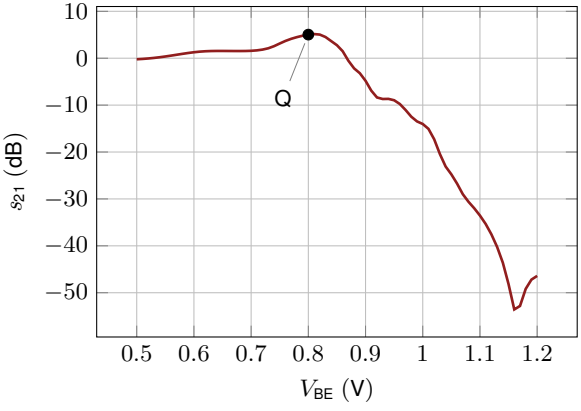
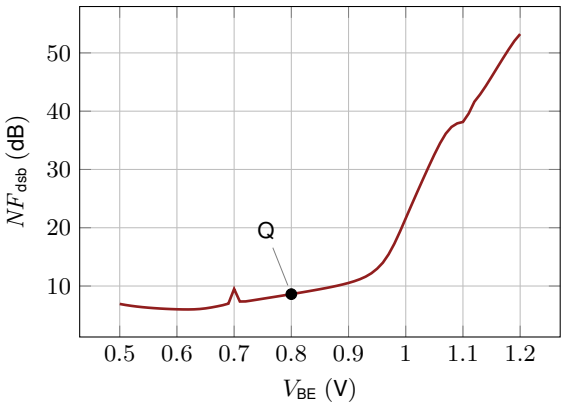
Operating Point: Switching Quad



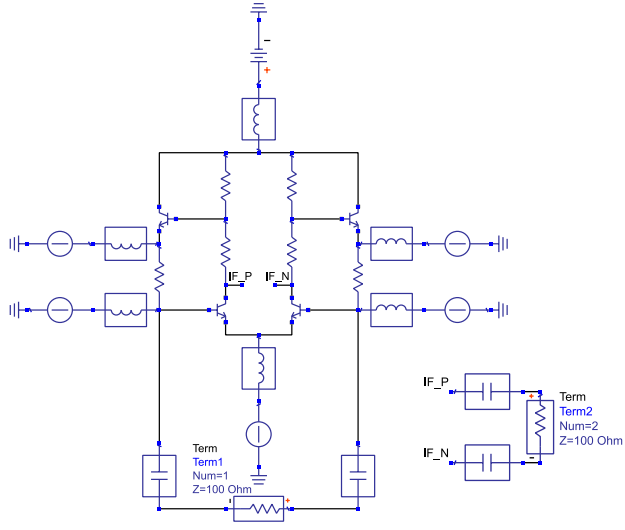


- Plotted for $f_{LO} = 135\,\text{GHz}$, $f_{RF} = 140\,\text{GHz}$
- Double-sideband noise figure NF_{dsb} (direct conversion mixer)
- Chosen operating point: $V_{BE} = 0{,}8\,\text{V}$

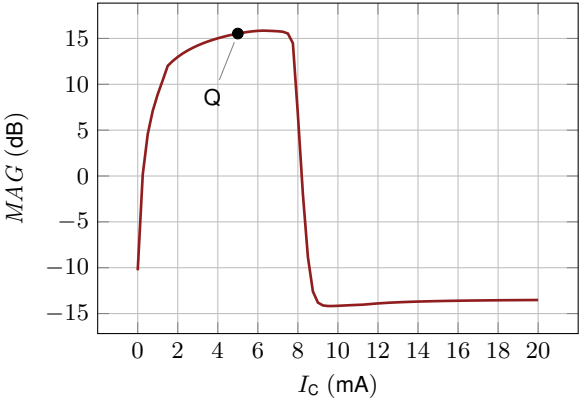
Operating Point: Transimpedance Amplifier

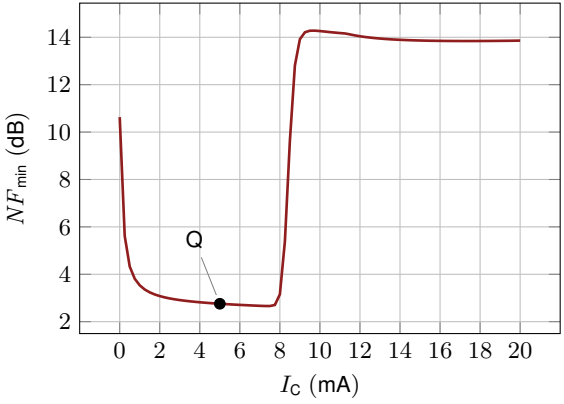
- Operation
  - Conversion of switched current to voltage, amplification
  - Modified Cherry-Hooper topology: decoupling of bandwidth and gain, modification for greater dynamic range

- Determination of operating point
  - Exact value of supply voltage not crucial
  - S-parameter simulation: Examination of maximum available gain (MAG) and minimum noise figure (NF_{min})
  - At this stage: only determination of operating point of bottom transistors



Operating Point: Transimpedance Amplifier

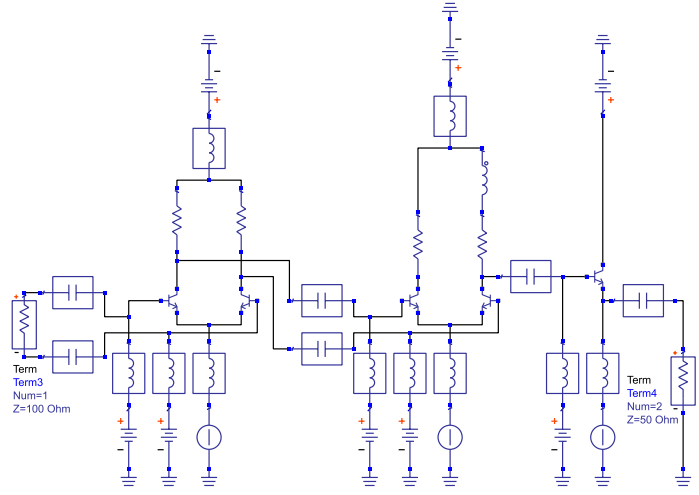




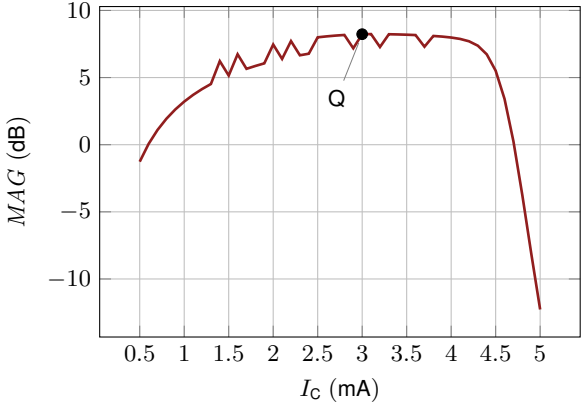
- Plotted for $f_{IF} = 20\,\text{GHz}$
- Chosen operating point: $I_C = 5\,\text{mA}$ (with multiplier of 10)

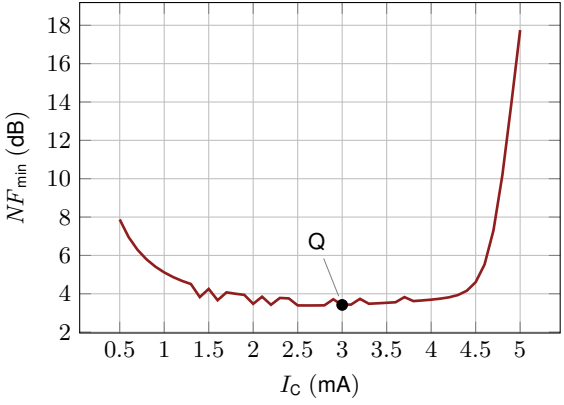
Operating Point: Buffer

- Operation
  - Amplification of signal
  - Comprises three stages: two differential amplifiers and an emitter follower
- Determination of operating point
  - Exact value of supply voltage not crucial at this point
  - S-parameter simulation: Examination of MAG and NF_{min}
  - **Note**: Adjustment with respect to linearity at the very end



Operating Point: Buffer

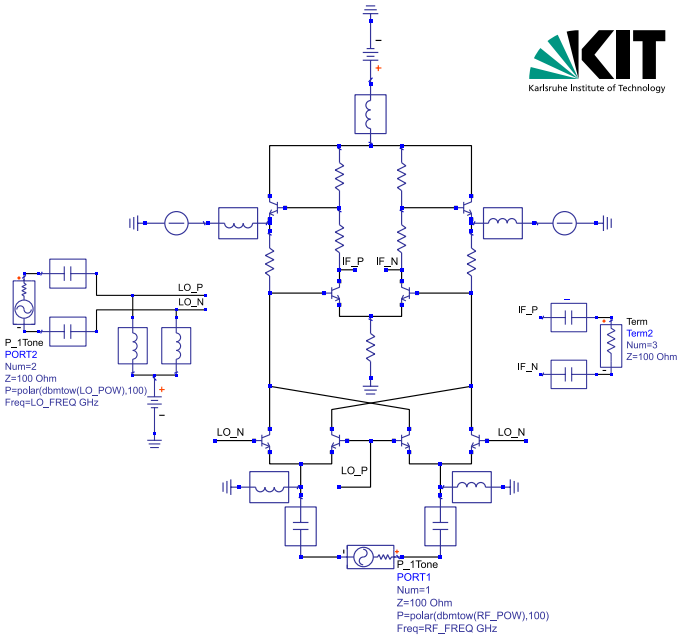




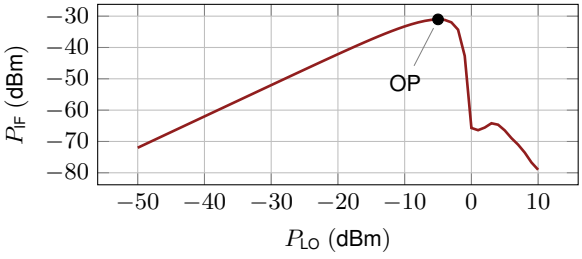
- Plotted for $f_{IF} = 20\,\text{GHz}$
- Chosen operating point: $I_C = 3\,\text{mA}$

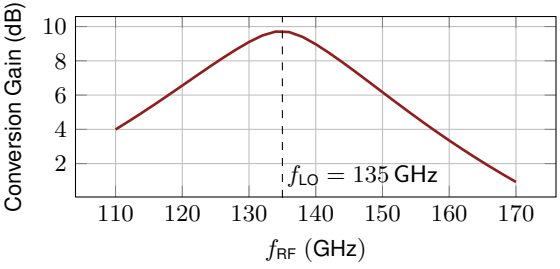
Integration: SQuad & TIA

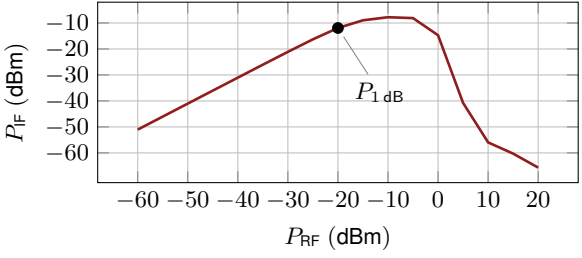
- DC coupling $\rightarrow$ Redesign of bias circuitry
- Supply voltage fixed to $2{,}5\,\mathrm{V}$ to not exceed breakdown voltage of transistors
- Examination using Harmonic-Balance simulation:
  - Conversion gain
  - $1\,\mathrm{dB}$ compression point ($P_{1\,\mathrm{dB}}$)

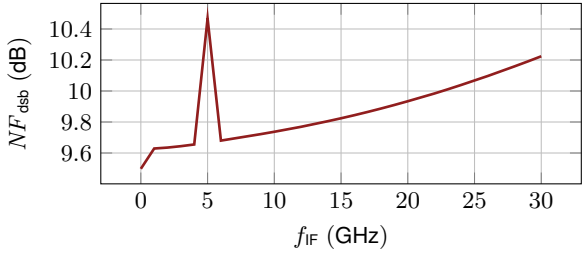


Integration: SQuad & TIA









Integration: SQuad, TIA & Buffer

- DC coupling $\rightarrow$ Redesign of bias circuitry
- Supply voltage fixed to $2{,}5\,\mathrm{V}$
- Examination using Harmonic-Balance simulation:
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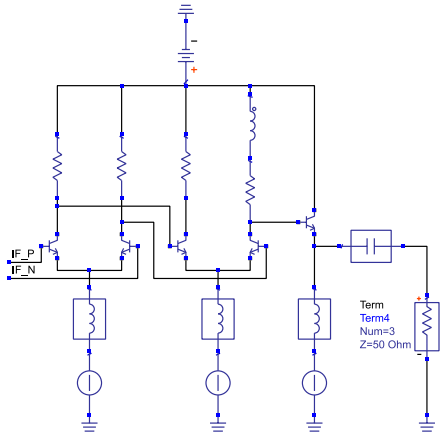
  - $1\,\mathrm{dB}$ compression point ($P_{1\,\mathrm{dB}}$)



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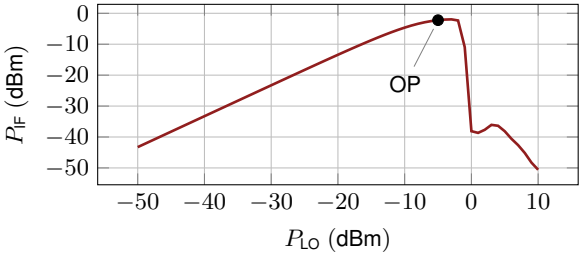
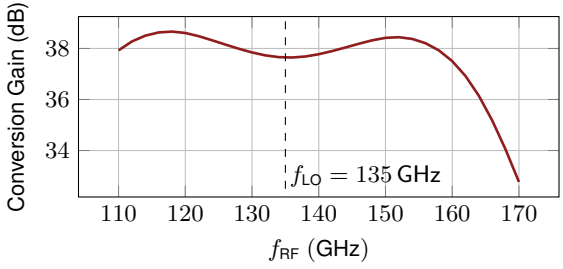
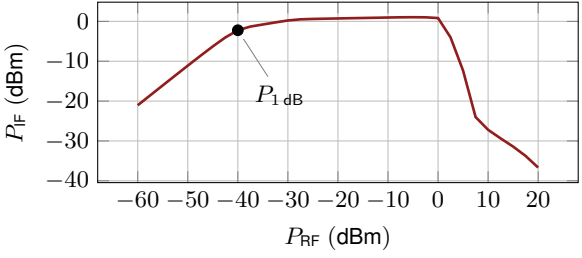
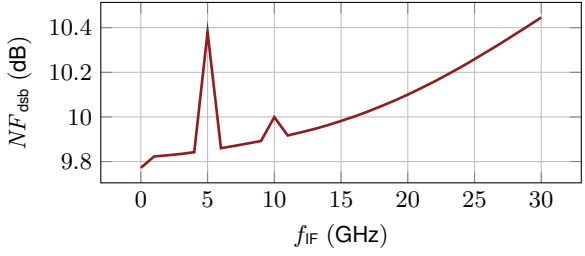
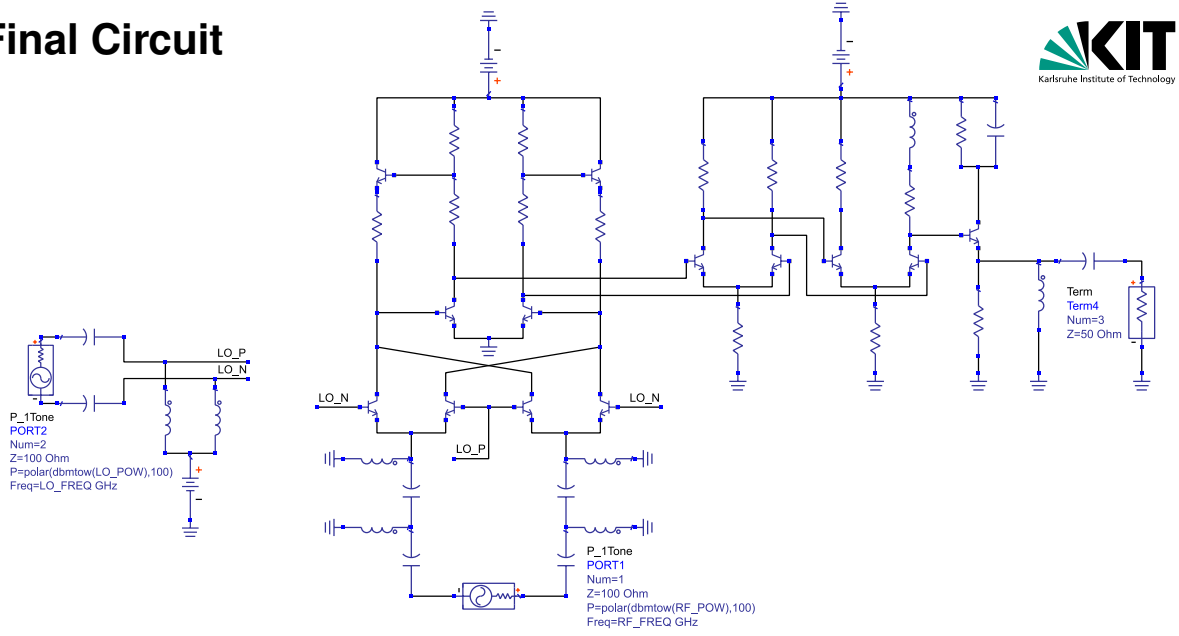








Final Circuit



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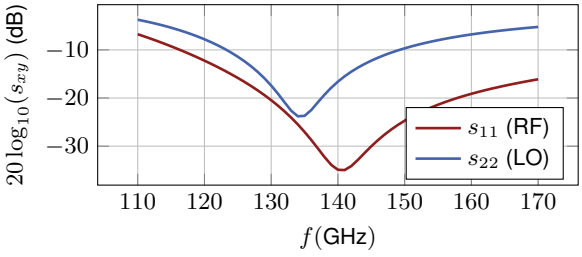

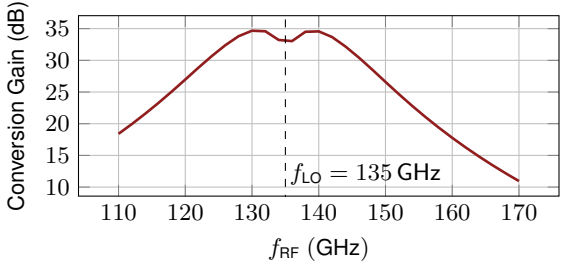

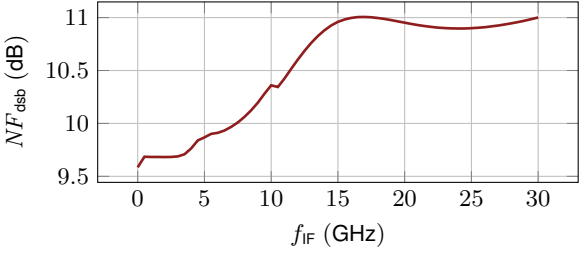

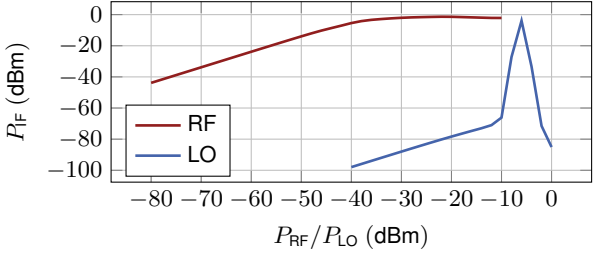

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Discussion & Conclusion

- General structure
  - Removal of g_m stage of Gilbert cell $\rightarrow$ more voltage headroom
  - High bandwidth TIA and inductive peaking $\rightarrow$ high bandwidth
  - Differential to single-ended conversion $\rightarrow$ dense chip-to-package transition
- Own simulations
  - Better results to be expected (technology with higher f_t, f_max, stability not considered)
  - Further investigation needed to determine whether unusual LO power behavior is problematic
  - Maybe better results by using current mirrors to set operating points of buffer instead of resistors
  - Maybe better results by replacement of discrete component matching networks by transmission line based ones
- Applications of this design
  - SiGe HBT technology integrable with CMOS $\rightarrow$ scalable, suitable for mixed-signal ICs
  - Ideal for electronic beam stearing in mm-Wave applications (because of small size, moderate noise figure)

Questions

Thank you for your attention!
Any questions?