A Broadband Zero-IF Down-Conversion Mixer in 130 nm SiGe BiCMOS for Beyond 5G Communication Systems in D-Band

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***Abstract*—This brief presents a broadband D-band down-conversion mixer in a cost efficient 130 nm SiGe BiCMOS technology with a f_t/f_{max} of 250/370 GHz from Infineon Technologies AG. The proposed mixer covers the entire D-band with a 32 dB peak conversion gain and a 3 dB bandwidth of 35 GHz at a measured noise figure between 9.5 and 12 dB in the specified band while consuming only 65 mW DC power. To achieve large RF and IF bandwidths and a low noise figure, the mixer design is based on a low-biased switching quad, which is loaded with a modified Cherry-Hooper transimpedance amplifier. The results, which are verified by measurements, are based on a detailed analysis of the transistor characteristics, broadband matching networks and an appropriate layout parasitic extraction. All interfaces to the circuit are designed single-ended for a dense chip-to-package transition. For this purpose, high performance Marchand baluns are used at RF- and LO-port, respectively. With a moderate noise figure and a low power consumption, the presented circuit meets the requirements for beyond 5G systems.**

***Index Terms*—6G, beyond 5G, broadband, communication, D-band, mixer, receiver.**

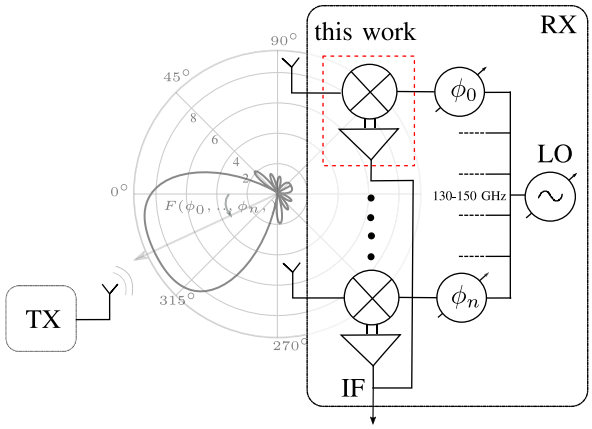

Fig. 1. System concept for a broadband phased array receiver with LO-path-phase-shifting.

I. Introduction

MMWAVE 5G meets the increasing demands of today's modern applications. Here, carrier frequencies between 28 and 40 GHz and sub-channel bandwidths up to 800 MHz are set to enable data-rates up to 10 Gbit/s. Following these trends for high-speed communication systems, the demand on even higher data rates and hence, even larger bandwidths and higher frequencies is already visible [1]. The advances in semiconductor processes with respect to f_t and f_{max} of the transistors, enable an efficient implementations of high performance communication components and systems [2], [3]. According to these trends, frequency bands beyond 100 GHz are promising for future communication systems with data rates on the 100 Gbps order [4]. They do not only offer a moderate atmospheric absorption and a high availability of high aggregate carrier bandwidths but also promote a high degree of integration for area efficient broadband couplers as well as antennas on-chip or efficient antenna-in-package solutions. Furthermore, on-chip transmission lines can be used for broadband matching networks with a reasonable area consumption. Due to a small effective antenna area, that increases free-space losses beyond 100 GHz, systems with high antenna gain and array factors are required for communication over several meters. Increasing array factors lead to smaller antenna beam widths, which need to be steered electronically in order to avoid the need for mechanical alignments between transmitter (TX) and receiver (RX). Consequently, large arrays, including more sub-receiver channels, lead to a high power consumption and heat development. The receiver front-end in Fig. 1, shows an adequate system concept, which is addressing these challenges. It features an array of power-saving

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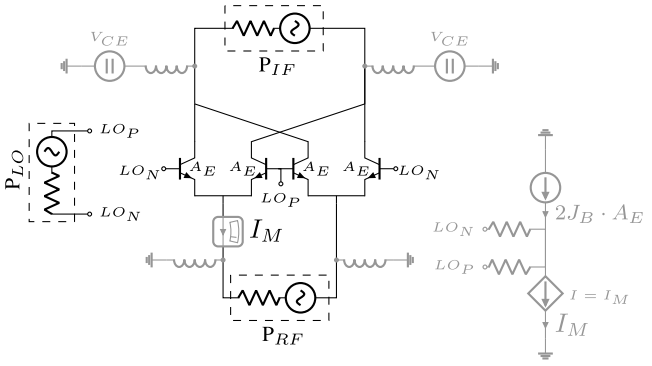

Fig. 2. Proposed simulation testbench for the switching quad. The bias components (gray) are used to control the bias current densities without influencing the RF-behaviour of the switching quad.

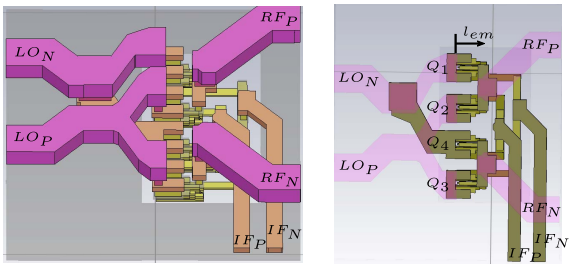

Fig. 3. 3D-view of the layout of the switching quad transistors.

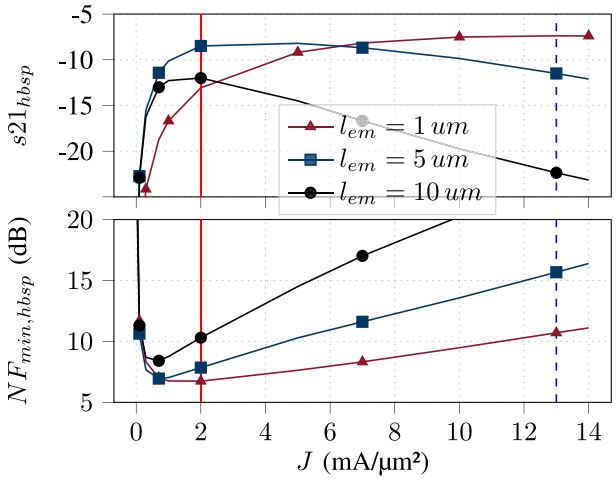

Fig. 4. Simulated double-sided NF and conversion gain ($s21_{hbsp}$) over bias current density J for a LO-power of 0 dBm.

mixer-first sub-receivers and phase-shifting in the local oscillator (LO) path. An advantage of the LO-path-phase-shifting approach is that the magnitude variation of the RF signal chain is low across all phase-shifting states [5]. Furthermore, the bandwidth requirement for the phaseshifter is relaxed. As, for the described architecture, the mixer becomes the first element in the sub-receiver chain, its key figures are bandwidth, a moderate noise figure, a low power consumption and a small input return loss. In the following sections, we present the design and measurement results of a receiver front-end with corresponding properties based on a broadband down-conversion mixer together with an IF buffer.

II. Mixer Design Considerations

For the proposed design we used Infineon's 130 nm SiGe technology - B11HFC. The available backend of line (BEOL) offers six copper based metal layers with two thick top-layers for RF routing purposes and a pad and redistribution aluminium layer. The technology features high-speed transistors allowing a f_t/f_{max} of 250/370 GHz with different transistor terminal configuration options [6]. For the down-conversion mixer we chose a current commutating double balanced mixer topology due to its inherent port-isolation property.

To investigate the noise performance of the circuit, we use the simulation testbench as depicted in Fig. 2. In order to isolate the noise contribution of the switching quad transistors, we omitted any kind of matching, buffer or additional load and connect it directly to the respective signal ports.

To find the optimal transistor size and current density J_{opt}, we parametrized the effective emitter area A_E and the corresponding bias current $I = J \cdot A_E$ with the bias circuitry, indicated in gray. Ideal inductors (L = 1 μH) serve as RF-block and provide the DC path to the circuit while keeping the collector potential V_{CE} adjustable and independent of the bias currents. Furthermore, we used Keysights Momentum electromagnetic (EM)-simulation results to include the impact of the core layout to the transistor performance, as shown in Fig. 3.

The layout is optimized for symmetry and allows the adaption of the emitter length l_{em} without changing its parasitic influence significantly and, thus, serves as a good approximation for the parametrization process. To keep the base resistance as small as possible, for minimum noise, we used the smallest emitter width and a transistor with two base terminals (BEBC configuration). Consequently, the emitter area was controlled via its length parameter.

In Fig. 4, Spectre-RF Harmonic-Balance S-Parameter (hbsp) simulation results for a LO-frequency of 135 GHz at 0 dBm power and a RF-frequency of 140 GHz are shown. The $s21_{hbsp}$ represents the power conversion gain to an IF of 5 GHz. The lower graph depicts the minimal noise figure of the switching quad again for an IF of 5 GHz. According to the results, an optimum for the current density of around 2 mA/µm^2 (red line) is visible. Compared to the current density for maximum transit frequency f_t of the transistor, marked as dashed (blue) line, the optimal bias point for this large-signal circuit is significantly lower. This is caused by a reduced influence of current-dependent shot- and thermal noise in the high- and low frequency domain, simultaneously.

As described in [7], for current commutating mixers, the non-ideal transit time within the states of the respective switching pair transistors, introduces additional thermal noise due to simultaneous non-zero transconductances of all switching transistors. Minimizing the transit time requires a square-wave LO-signal and thus, odd harmonics of the LO fundamental frequency. At D-band frequencies, these lie beyond the transit-frequency of the transistors and are attenuated strongly. Hence, for sub-THz circuits, applying enough LO-power is the option to further minimize the influence of this effect. Simulations of the presented circuit confirm this fact as shown in Fig. 5.

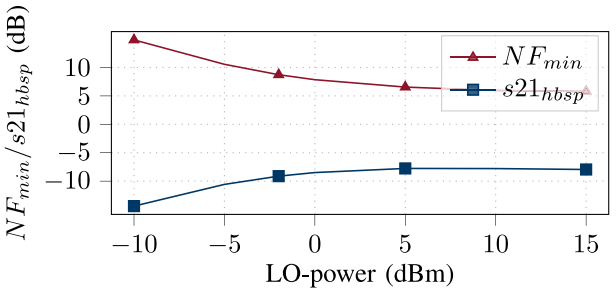

Fig. 5. Simulated double-sided minimal NF and conversion gain ($s21_{hbsp}$) over LO-power for a transistor with 5 µm emitter length.

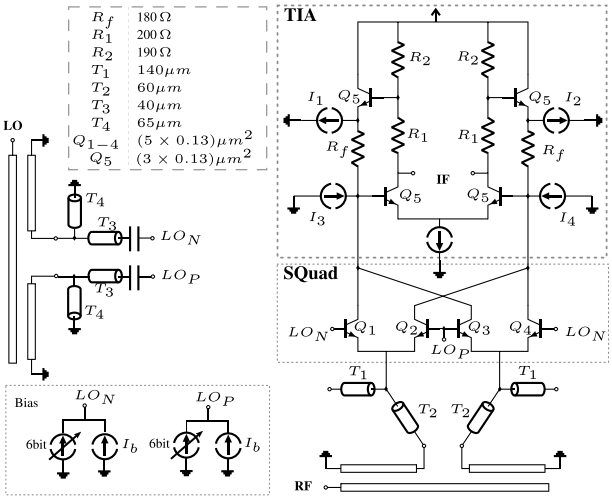

Fig. 6. Schematic of the proposed mixer core cell.

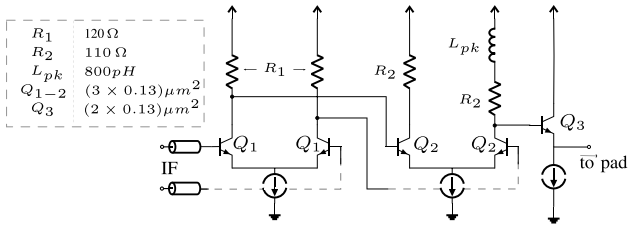

Fig. 7. Schematic of the IF buffer with inductive peaking.

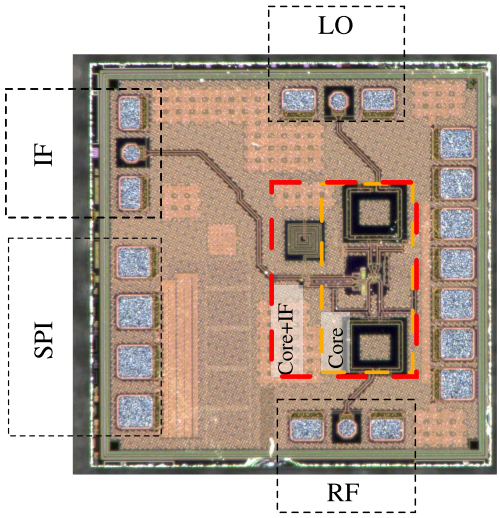

Fig. 8. Mircograph of the mixer test die. The outer dashed square indicates the mixer including IF buffer with a physical size of 360x530 µm, the inner dashed square is the mixer core with a size of 310x530 µm.

According to the presented analysis results, an emitter length of 5 µm and a current density of 2 mA/µm^2 were chosen for the switching quad in the following design.

III. Mixer Implementation

Fig. 6 shows the schematic of the double balanced mixer core loaded by a modified Cherry-Hooper transimpedance amplifier (TIA) [8].

The frequency conversion within the mixer core is performed by the current commutating switching-quad (SQuad), which is composed of four npn-transistors as described in the previous section. In contrast to a conventional Gilbert cell, omitting the Gm-stage in this design provides more voltage headroom for the DC coupled IF buffer, and thus, the system can be operated by a 2.5 V supply voltage. Furthermore, the described bias point for optimal noise performance of the switching quad could be implemented easily by introducing the current sources I_1-I_4. Additionally, they provide a low DC current through the feedback resistor R_f, which enables a smaller physical layout in order to keep parasitic effects in the layout as small as possible. Furthermore, the optimal bias points and transistor sizing of the switching quad and the TIA are designed almost independently, i.e., therefore optimized regarding bandwidth, noise figure and conversion gain. The base terminals of the switching quad transistors are biased with two digital adjustable current sources at the LO_N and LO_P terminals, respectively, in order to fine-tune the bias points for the measurement. The digital interface is realized via SPI on-chip. For a wideband RF matching from 110 GHz to 160 GHz (see Fig. 9) the matching networks are designed in a transmission line based differential L-Type network. Due to high isolation in double balanced mixers, the matching networks for the LO- and RF-port can be designed independently. To present the differential signal to the double balanced mixer core, two synthesized Marchand baluns are used, which we describe in detail in [9]. They provide a very broadband 100 Ω differential interface to the circuit compared to common transformer based baluns. For the EM-simulation of the transmission lines and the Marchand balun Sonnet's EM-simulator was used.

To provide a broadband signal amplification and to anticipate package losses, the mixer core is followed by a three-stage baseband amplifier including a differential to single-ended conversion as shown in Fig. 7. To enhance the IF bandwidth by compensating bandwidth-limiting parasitic transistor- and layout-introduced effects, the second stage comprises the inductor L_{pk} for inductive peaking. Fig. 8 shows the implementation of the test die including RF pads and SPI interface. All chip interfaces are designed single-ended to enable a dense chip-to-package transition, as it is required in compact large array systems.

IV. Experimental Results

The small signal response of the inputs in D-band have been determined using a Keysight PNA-X N5247B together

TABLE I
COMPARISON WITH PUBLISHED STATE-OF-THE-ART FREQUENCY DOWN-CONVERTING CIRCUITS BEYOND 100 GHz. SIMULATION RESULTS ARE MARKED WITH *

	[10] 2017	[11] 2019	[12] 2017	[13] 2019	[14] 2016	[15] 2016	this work
Technology	SiGe 130nm BiCMOS	SiGe 130nm BiCMOS	SiGe 130nm BiCMOS	FDSOI 22nm CMOS	SiGe 130nm BiCMOS	65nm CMOS	SiGe 130nm BiCMOS
ft/fmax [GHz]	300/500	300/500	300/500	240/230	250/300	-	250/370
NF [dB]	18(SSB)	12(DSB)	10.7(DSB)	8.5*(DSB)	15*(SSB)	33(-)	9-11(DSB)
DC power [mW]	500	100	122	198	115	6	65
Conversion gain [dB]	25.3	14	47	12	21	-11	32
f[GHz] /3 dB BW [GHz]	240/55	190/80	190/35	135/22	140-170/30	120/14	110-170/35
RF- bandwidth [%]	23	44	18.4	16.3	19.3	11.7	25
Chip area [mm^2]	-	-	-	-	0.7	-	0.2
Integration	multiplier mixer IF-buffer	LNA LO-driver mixer IF-buffer	LNA LO-driver mixer IF-buffer	LNA LO-driver IQ-mixer IF-buffer	LO-driver mixer IF-buffer	mixer	mixer IF buffer

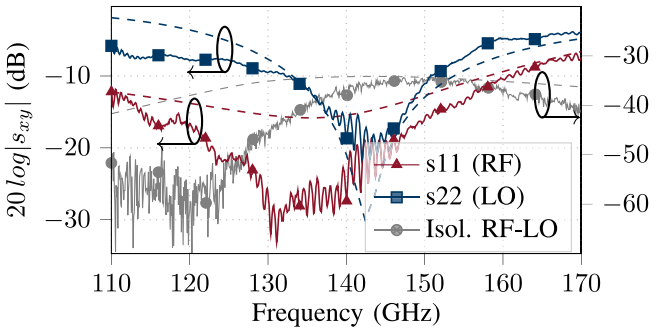

Fig. 9. Measured (solid) and simulated (dashed) S-parameters of the mixer.

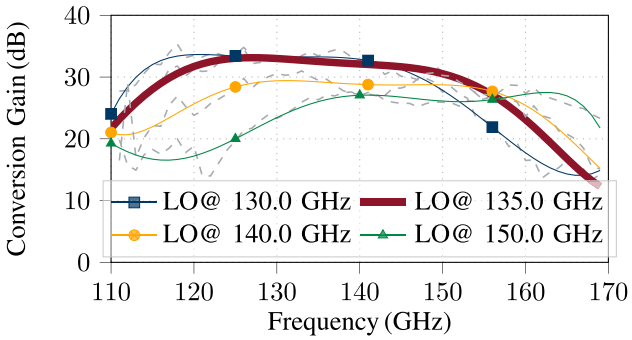

Fig. 10. Power conversion gain of the mixer over RF frequency. Tuning the LO frequency enables to cover the entire D-Band with a conversion gain ≥ 20 dB.

with VDIs VNAX D-band extenders. As depict in Fig. 9, the mixer presents a return loss ≤ −10 dB within a bandwidth of 110 to 160 GHz for the RF input signal. The return loss of the LO-port is matched from 132 GHz to 150 GHz, which enables a wide tuning range. LO and RF ports are isolated against each other more than 34 dB as shown in Fig. 9. Due to a detailed parasitic extraction, the measurements are in good agreement with the corresponding simulations.

To measure the large signal behavior, VDI's VNAX D-band extender were used as signal sources, which enable to control the output power by a mechanical attenuator. The RF signal spectrum has been investigated using a PM5

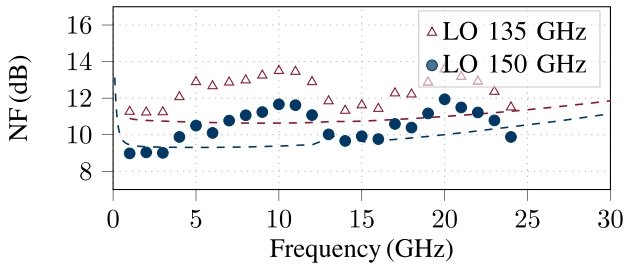

Fig. 11. Measured and simulated (dashed) noise figure of the mixer for different frequencies at −6 dBm LO power over IF.

Erickson powermeter and a PXA N9030A spectrum analyzer together with VDI's SAX spectrum analyzer extender. To increase the measurement accuracy, all power levels as well as losses within the probing equipment have been determined carefully. As shown in Fig. 10, the mixer yields a (power) conversion gain of 32 dB within a 3 dB bandwidth from 116 GHz-151 GHz. Furthermore, by tuning the LO-frequency, a large frequency range within the D-band can be covered. Communication systems using multiple frequency sub-channels, like OFDM, may also benefit from the bands outside of the flat area and thus, take advantage of the entire D-band for high speed data transfer. According to Shannons channel law, next to bandwidth, low noise is a key feature for a maximum achievable data-rate. Due to a strong frequency dependency of the excess-noise-ratio (ENR) of the available noise source, the Y-factor method could not be applied properly for the broad IF band. Instead, the noise figure has been determined using the Gain Method. At the input, a 50 Ω termination resistor was applied at a room temperature of 295 K. A given bandwidth B of the spectrum analyzer yielding an input noise power (in dBm) of:

$$N_0 = 10\,log_{10}(kBT_0 \cdot 1000) \tag{1}$$

After the determination of the conversion gain G, the noise factor of the DUT yields:

$$F = \frac{SNR_i}{SNR_o} = \frac{\frac{S_i}{N_{0,in}}}{\frac{S_o}{N_{0,out}}} = \frac{N_{0,out}}{GN_{0,in}} \tag{2}$$

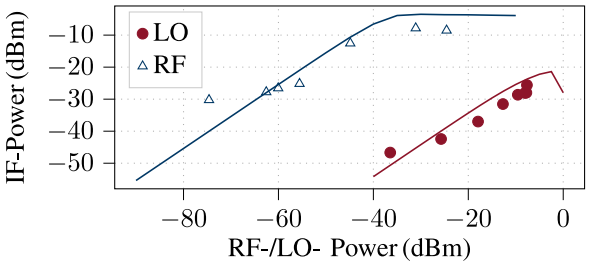

Fig. 12. Compression curves of the mixer circuits at an IF of 5 GHz. The results with triangular marker show the IF power over the applied input power with a fixed LO power of −10 dBm. The measurement points with a cyclic marker are mapping the IF power to the applied LO power with a fixed RF input power of −60 dBm.

Although using the "Gain Method" comprises some uncertainties, measurements confirm the simulation results as shown in Fig. 11. Fig. 12 shows the measured input referred compression point of −41 dBm, which is caused by the high gain of the IF amplification. However, due to the high free-space losses in D-band, very low input levels are expected even for short distances. The simulated optimum conversion gain and noise figure is reached for a LO power of −2 dBm. The maximum available output power of the measurement equipment is −6 dBm, but again measurements confirm the simulation results within the measurable range.

The whole circuit, including biasing components, consumes 26 mA at a supply voltage of 2.5 V. The switching quad is biased with a current of 5 mA, so that the main power-consumption is assigned to the broadband IF amplification.

V. Conclusion

Within this brief a broadband zero-IF D-band down-conversion mixer with a 3 dB bandwidth of up to 35 GHz is presented. Here, the presented transistor sizing and biasing analysis for a optimal noise performance is a key enabler for a low noise figure, a very broadband RF input matching, and a large 3 dB bandwidth for the conversion gain. By steering the LO-frequency, RF signals within the entire D-band can be converted with a conversion gain $\geq$ 20 dB. To compare this measurement results, Table I summarizes recent state-of the-art receiving systems with frequencies beyond 100 GHz. The proposed work shows overall best results with respect to relative bandwidth, noise figure, power consumption and area demand and thus, fulfills the key requirements for the challenges of beyond 5G wireless communication systems.

Acknowledgment

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